Laboratoire ESYCOM

le cnam cnrs Université Gustave Eiffel

PhD offer in electronics/mechatronics/electrical engineering

Design and characterization of electrostatic micro-actuators for capacitive adiabatic computation

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1 Scientific description

Current mainstream computation systems are based on CMOS technology. Performing logic operations using CMOS logic gates implies to charge and discharge capacitors that are inherent to the physics of (MOS)FET transistors. This is done by connecting the transistors to steady voltage levels provided by the power supply. But (i) the charging/discharging is inefficient (ii) the invested energy on charge is forever lost on discharge. As a result, state-of-the-art CMOS-based computation technologies consume about $1000\,k_{\mathrm{B}}T$ per operation (a few attojoules per op. at $T = 300\,\mathrm{K}$). This figure is orders of magnitude above the Landauer limit [Lan61]. Therefore, research on ultra-low power electronics and ICT (information & computing technology) investigates new paradigms in order to drastically decrease the power consumption of computation devices. Capacitive adiabatic computing is one such paradigm.

Capacitive adiabatic computing aims at implementing boolean operations by using electromechanical variable capacitors as logic gates, in place of transistors. The charging is efficient because the electromechanical dynamics of each logic gate are controlled so as to minimize the dissipated energy. Furthermore, the capacitive design of the gates allows to recover the energy invested for a given change of state of the logic gate, during a subsequent change of state of the same gate. The reference [PGH21] describes the capacitive computing paradigm in more details.

Throughout its PhD, the candidate will have to cleverly design the microelectromechanical (MEMS) systems used to implement the capacitive logic gates. Given the adiabatic computing context, the design will aim at minimizing the energy cost, while ensuring the logic functionality at the system-level. The designs will be fabricated in bulk silicon in the lab's cleanroom. The candidate will then run thorough experimental characterizations of the fabricated devices to validate functionality, assess the attainable consumption levels, and refine/fit the analytical models. In collaboration with the G2ELab (see below), the candidate will assess the possible benefit of replacing air/vaccum with fluids as the electromechanical capacitors dielectric material. This results in lower actuation voltages, and hence electrical dissipation. The design will have to balance this benefit with the necessarily larger viscous losses.

In all, a core objective of the PhD is to build a working prototype of a capacitive logic gate – possibly through several iterations – at ultra-low power consumption levels, while ensuring operation at a reasonable speed. Depending her/his interests and advancement, the PhD student can complete his/her work by the study of the power supply circuits for adiabatic logic gates ("power clock"), or of the cascading of several gates for more complex logical operations.

This work is expected to have a strong impact by showing that the energy consumption can be decreased by one or several order of magnitudes using the capacitive adiabiatic computing paradigm, while relying on existing MEMS technology.

2 Academic setting

The recruited PhD candidate will carry out her/his research at the ESYCOM laboratory, located in the Universté Gustave Eiffel campus. The laboratory has been a major international actor in the research on mechanical/electrical/thermal/radiofrequency micro-energy harvesting, management and usage, for more than a decade. The laboratory works on all aspects of micro-energy systems: system-level modeling, simulation, fabrication, and characterization. The laboratory has access to a state-of-the-art 600 m^2 cleanroom for the fabrication of the designed devices and their electrical interfaces. Experimental facilities located within the laboratory allows the characterization of the fabricated devices.

This PhD work takes place within the "zerOuate" project, selected for funding by the French national agency for research (ANR) after a competitive process. The PhD student will regularly travel to and collaborate with the others labs of the consortium, namely, G2ELab, CEA-LETI (both located in Grenoble, France), and LAAS-CNRS (located in Toulouse, France).

3 Candidate profile

The ideal applicant has a master's degree in electrical engineering, electronics, or mechatronics. Students with a mechanical engineering or physics degree are also encouraged to apply. The applicant should have a good foundation on the theoretical aspects of engineering, while enjoying the practical side. Prior experience in MEMS/circuit design, simulation, and characterization, although a plus, is not necessary.

Fluency in English is a must, both spoken and written. French is a plus but is not mandatory.

4 Practical information

The PhD can start as soon as possible, and before January 2022 (included). The PhD has an exact duration of three years (36 months).

The PhD is fully funded for its whole duration, with a monthly compensation of ∼1600 euro net salary. This salary can increased by up to about 300 euros/month if the PhD candidate is additionally recruited for a teaching assistant position starting from fall 2022 (max. of 64 hours/year teaching duty). Travel costs (to conferences, collaborators' laboratories, . . .) are covered by the funding.

The candidate will conduct his/her research at the ESYCOM laboratory, located in Champs-sur-Marne, Paris metropolitan area. The center of Paris is at about 25 minutes using public transportation.

The university can help foreign PhD students to find housing at an affordable price.

5 Contact

Prospective applicants have to send their application (at least a cover letter + a resume) to Armine Karami (contact details on top of 1st page). They can also reach out to hear more about the subject.

6 Bibliography

[Lan61] R. Landauer. "Irreversibility and Heat Generation in the Computing Process". In: *IBM Journal of Research and Development* 5.3 (1961), pp. 183–191. DOI: 10.1147/rd.53.0183.

[PGH21] Y. Perrin, A. Galisultanov, L. Hutin, P. Basset, H. Fanet, and G. Pillonnet. "Contact-Free MEMS Devices for Reliable and Low-Power Logic Operations". In: *IEEE Transactions on Electron Devices* 68.6 (2021), pp. 2938–2943. DOI: 10.1109/TED.2021.3070844.